REMARKS

Claim 2 has been cancelled. Claims 1 and 3 have been amended. Claims 11 – 17 have been added. Claims 1, 3 and 11-17 are pending. In view of the above amendments and remarks below, the Applicant requests allowance of all claims.

Claim Rejections – 35 U.S.C. 112

In the Office action, claim 2 was rejected for containing informalities. The rejection is moot because claim 2 has been cancelled.

Claim Rejections – 35 U.S.C. 102

In the Office action, claim 1 was rejected as being anticipated by U.S. Patent No. 5,656,522 to Komori et al. Claim 1 has been amended to clarify that the oxide film is formed simultaneously and selectively in at least two locations. The oxide film is selectively formed (1) on the floating gate of the non-volatile memory cell transistor, and (2) as a gate insulating film layer of the MOS transistor. The selective formation of the oxide layer is described in the specification, for example, at page 9, line 21 to page 10, line 1. No new matter has been added.

In contrast, in the Komori device, the film is not selectively formed, instead a "the film (9A) is formed on the entire semiconductor substrate . . . including the upper surfaces of the gate insulating films (8)." See col. 8, lines 33-36. In the present application, when a tunneling insulating layer is subsequently formed over the entire upper surface, the previous selective formation of the gate insulating film simultaneously with the floating gate insulating film provides a MOS gate insulator that can withstand a higher gate voltage without the necessity of an additional thermal oxidation step.

Thus, Komori et al. does not teach or suggest simultaneously and selectively forming the oxide film on the floating gate of the non-volatile memory cell transistor and a thick gate insulating film of the MOS transistor in a single thermal oxidation step as recited in amended claim 1. Claim 1 is not anticipated by Komori et al. because Komori et al. does not claim each

and every element of claim 1. Applicant respectfully requests withdrawal of the 35 U.S.C. 102(b) rejection of claim 1.

Claim Rejections – 35 U.S.C. 103(a)

Claims 2 and 3 have been rejected as being unpatentable over Komori et al. as applied to claim 1, in view of U.S. Patent No. 6,165,845 to Hsieh et al. The rejection of claim 2 is moot because claim 2 has been cancelled. Claim 3 has been amended to depend from new claim 11.

Claim 11, like claim 1, recites that the oxide film is formed "simultaneously and selectively" in at least two locations. Claim 11 also recites forming a tunneling insulating film on the gate insulating film. Thus, there is a stacking of the tunneling insulating film on top of the gate insulating film. Hence, a thicker gate insulating film is formed, which increases the withstanding voltage. Simultaneously and selectively forming the oxide film on the control gate and forming the thick gate insulating film can increase the MOS transistor withstanding voltage without the necessity of an additional thermal oxidation step.

Neither Komori et al. or Hsieh et al. either alone or in combination teach or suggest simultaneously and selectively forming the oxide film on the floating gate of the non-volatile memory cell transistor and a gate insulating film of the MOS transistor in a single thermal oxidation step and subsequently forming a tunneling layer on top of the gate insulating layer as recited in claim 11. None of the cited references suggests recognition that an increase in gate insulating voltage may be achieved by forming a gate insulator by stacking an oxide film on a gate insulating film.

In view of the foregoing remarks, Applicant respectfully requests withdrawal of the 35 U.S.C. 103(a) rejection of claim 3.

Conclusion

Applicant respectfully requests allowance of all claims.